REPORT OF
DEPARTMENT OF DEFENSE
ADVISORY GROUP ON ELECTRON DEVICES

SPECIAL TECHNOLOGY AREA REVIEW
ON
MICROWAVE PACKAGING TECHNOLOGY

FEBRUARY 1993

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION
WASHINGTON, D.C. 20301-3140

THIS REPORT IS A PRODUCT OF THE DEFENSE ADVISORY GROUP ON ELECTRON DEVICES (AGED). THE AGED IS A FEDERAL ADVISORY COMMITTEE ESTABLISHED TO PROVIDE INDEPENDENT ADVICE TO THE OFFICE OF THE DIRECTOR OF DEFENSE RESEARCH AND ENGINEERING. STATEMENTS, OPINIONS, RECOMMENDATIONS, AND CONCLUSIONS IN THIS REPORT DO NOT NECESSARILY REPRESENT THE OFFICIAL POSITION OF THE DEPARTMENT OF DEFENSE.

PREFACE

Progress has been made in recent years in the area of microwave integrated circuit design, fabrication, testing and affordability. However, there are dominant technical issues that remain to be resolved in the development of microwave (MW) and millimeter wave (MMW) multichip module packaging. The purpose of this study was to examine this emerging technology that is of great importance for both defense and commercial applications and to help the DoD, industry and academia develop an appropriate investment strategy to develop complex, lightweight, and high density electronics modules using microwave, digital, and photonic technologies.

The study was performed by the Department of Defense's Advisory Group on Electron Devices (AGED)—specifically by AGED's Working Group A which is responsible for coordinating microwave device development for the Department of Defense. This report contains information that resulted from Working Group A's Special Technology Area Review (STAR) of Microwave Packaging Technology that was held on 18-19 June 1992 at the Georgia Institute of Technology, Atlanta, GA.

The editor appreciates the efforts of all the contributors—listed on the next page—who participated in the review and in writing the report. Thank you especially to the Solid State Electronics Directorate, Microwave Division, Wright Laboratory, Dayton, OH for their kind help in writing this report. Additionally, the support of Dr. John MacCallum, Office of the Director of Defense Research and Engineering (Advanced Technology), has been important to this effort.

Becky Terry
Palisades Institute
for Research Services, Inc.
(AGED Secretariat)
Arlington, VA

CONTRIBUTORS

Dr. John M. MacCallum, Jr.
Executive Director, Advisory Group on Electron Devices
ODDRE/AT, The Pentagon
Washington, DC

Dr. Joseph A. Saloom
Chairman, Working Group A (Microwaves)
Boxford, MA

Barry R. Allen
TRW, Inc.
Redondo Beach, CA

John Bedinger
Texas Instruments
Dallas, TX

Robert Bierig
B&B Technology
Hopkinton, MA

Eliot D. Cohen
DARPA
Arlington, VA

Joseph M. Colussi
Navy Air Warfare Center
Warminster, PA

William J. Edwards
Wright Laboratory
Wright-Patterson AFB, OH

Michael Flanders
Coors Electronic Package Co.
Chattanooga, TN

Vladimir G. Gelnovatch
USA Research Laboratory
Fort Monmouth, NJ

Achim Hill
Compact Software
Paterson, NJ

Robert T. Kemerley
Wright Laboratory
Wright-Patterson AFB, OH

Charles Krumm
Hughes Aircraft Co.
El Segundo, CA

Ronald J. Naster
General Electric Co.
Syracuse, NY

Peter Parrish
EEsof, Inc.
Westlake Village, CA

Richard Perko
M/A-COM, Inc.
Burlington, MA

Barry S. Perlman
USA, Research Laboratory
Fort Monmouth, NJ

Kurt Shalkhauser
NASA Lewis Research Center
Cleveland, OH

Elissa Sobolewski
DARPA
Arlington, VA

Carl Thomas
Rome Laboratory
Griffiss AFB, NY

John R. Tyler
Avantek, Inc.
Santa Clara, CA

James L. Vorhaus
Avantek, Inc.
Santa Clara, CA

CONTENTS

I. EXECUTIVE SUMMARY

Microwave (MW) and millimeter wave (MMW) multichip module (MCM) packaging is an emerging technology that is of great importance for both defense and commercial applications. Military applications such as radar, electronic warfare, communications, and smart munitions and commercial applications such as communications, direct broadcast satellite, cellular telephone, and automotive electronics all require MW and/or MMW electronics. The spectrum of needs ranges from low volume, high performance electronics to high volume, low cost applications. A significant aspect of realizing these components and systems will be the development of a broad range of packaging and interconnect technologies that have the required reliability and environmental protection and are affordable and applicable to both the military and commercial sectors.

With the rapid progress made in monolithic microwave integrated circuit (MMIC) development as a result of substantial investment made by the DoD, the cost of design, fabrication, and test has significantly dropped. MMIC technology is being actively transitioned to operational and new military systems. The pacing issue today is that packaging of multichip modules is a major cost driver.

As a result of the system needs and the present day technology limitations, the Advisory Group on Electron Devices (AGED), Working Group A (Microwave), conducted a "Microwave Packaging Technology" STAR during 18-19 June 1992 at the Georgia Institute of Technology, Atlanta, GA. Information resulting from the STAR will be used by the Department of Defense (DoD), industry, and academia to develop an improved investment strategy for MW and MMW packaging technology. STAR emphasis was placed on the application of advanced packaging and interconnect technology to high performance phased array antennas and other complex multichip, multipackage systems. The scope of the technology encompasses array subassemblies, antenna elements, RF components, RF/digital/optical interconnects, control circuits, and thermal management assemblies. The subject report summarizes the information discussed at the STAR and provides recommendations for MW and MMW packaging technology investment. Technology findings and recommendations are made for the areas of materials; die; multilayer structures; metal and metal matrix housings; assemblies of MCMs; manufacturing technology; packaging design, modeling and simulation; testing; and specifications and standards. "Batch fabrication" techniques must be developed at all levels of manufacturing to significantly impact overall system affordability. Technical performance advances over and above a linear extension of current packaging technology are required to meet future system requirements that impose three dimensional size constraints, light weight, adverse thermal environments, and long mission life operation.

With ever increasing competition for fewer and fewer resources, it is very important to evolve a well planned, focused MW/MMW MCM investment strategy. Section V,A of the report summarizes the current exploratory development (6.2), advanced development (6.3), and manufacturing technology (7.8) packaging program investment. Included in the information are programs that are under contract and those planned to start in FY93. In Section V,B, focused investment recommendations are proposed for future work. The basis for the recommendations is the STAR information contained in the Appendix of the report (STAR viewgraphs and

packaging materials information tables). Specific areas recommended for investment, over the next 4 years, are listed in Table 1 and discussed below.

Table 1. Packaging Technology Areas Recommended for Investment

AREA	INVESTMENT (Person Years)
Materials Development & Characterization:	28
Packaging Design, Modeling & Simulation:	60
Advanced Structures & Interconnects:	60
MMIC Coatings:	24
Manufacturing Technology for Affordable Multiple Assemblies of MCMs:	51
Total Investment (Over 4 years)	223

RECOMMENDATIONS:

1) **Materials Development and Characterization**: This area of investment concerns the development of a comprehensive and reliable database and data models of MW and MMW material properties, component properties, and interface properties for package design and fabrication

RESOURCES REQUIRED: 7 person years/year for 4 years

2) **Packaging Design, Modeling and Simulation**: A program consisting of 3 Phases is proposed. In Phase 1, user requirements will be defined and assessments of available tools will be conducted. Case studies involving definition, application, and assessment shall be made. In Phase 2, development and integration of tools, databases, framework models, and package design advisors will be conducted. In the final Phase, the developed CAE system will be evaluated by use in the design, modeling and simulation of a broad range of MW and MMW MCMs.

RESOURCES REQUIRED: 15 person years/year for 4 years

3) **Advanced Structures and Interconnects**: Three key areas of investment are recommended: Multilayer Structures, Metal Matrix Housings, and Plastic Packages. The Multilayer Structures effort will be focused on the manufacturability of MW/MMW structures with special focus on thermal management performance.

RESOURCES REQUIRED: 8 person years/year for 3 years per multilayer structure

The second area concerns the development of metal matrix composite housings with focus on dimensional tolerances, incorporation of feed throughs, and hermeticity.

RESOURCES REQUIRED: 8 person years/year for 3 years per material

The recommended investment in plastic packages concerns the development and evaluation of injection molded and premolded plastic packages for MW/MMW military applications.

RESOURCES REQUIRED: 4 person years/year for 3 years

4) **MMIC Coatings**: The recommended investment in this area is to develop and evaluate coating materials for MMIC chips. Emphasis will be placed on developing coatings that are applied at the wafer level, are compatible with MMIC processing, and are compatible with a variety of housing materials.

RESOURCES REQUIRED: 8 person years/year for 3 years

5) **Manufacturing Technology for Affordable Multiple Assemblies of MCMs**: A multifaceted program will be conducted. In Phase 1, the design of a subarray assembly will be conducted in which the performance, thermal management electrical interfaces, and other critical array requirements will be determined. In Phase 2, various subarray materials, processing technologies, chips, components, interconnections, and packaging will be developed. An integral part of the work will be to develop the associated manufacturing technology needed to demonstrate the subarray assembly in a flexible volume manufacturing environment. In Phase 3, a small number of subarrays will be built to demonstrate the subarray manufacturing technology.

RESOURCES REQUIRED: 17 person years/year for 3 years

II. INTRODUCTION

Electronic packaging technology is a pervasive and enabling technology that enhances system performance for both defense and commercial applications. It may well establish the competitive level and survivability of both military systems and the U.S. electronics industry.

The focus of this report centers on the technologies needed for the assembly of a number of microwave and millimeter wave integrated circuit chips into a package and the assembly of a number of these packages into higher level assemblies for a broad range of system applications. Such multichip assemblies may contain digital and possibly optoelectronic components that are integrated with the microwave (MW) or millimeter wave (MMW) integrated circuits (ICs). Packaging is defined in a broad sense to not only include the materials and technologies required to provide electronic components with physical protection and electronic connections, but also to include system architecture and partitioning approaches, power management, thermal management, data flow and timing, and input/ output interfaces.

The motivation for focusing and strengthening the US investment in electronic packaging technology is the potential for significant advancements in system performance and affordability. Today, packaging is a major cost driver. Issues of performance, reliability, size, weight, environmental stress, maintainability, and cost must be simultaneously addressed in developing and manufacturing the appropriate packaging technology.

Microwave and millimeter wave multichip module (MCM) packaging is an emerging technology that is of great importance for both defense and commercial applications. Military applications such as radar, electronic warfare, communications, and smart munitions; and commercial applications such as communications, direct broadcast satellite, cellular telephone, and automotive electronics, all require MW and/or MMW electronics. The spectrum of needs range from low volume, high performance electronics to high volume, low cost applications. A significant aspect of realizing these components and systems will be the development of a broad range of packaging and interconnect technologies that have the required reliability and environmental protection and are affordable by and applicable to both the military and commercial sectors.

As a result of system needs and present day technology limitations, the Advisory Group on Electron Devices (AGED), Working Group A (Microwaves), conducted a "Microwave Packaging Technology" STAR during 18-19 June 1992 at the Georgia Institute of Technology, Atlanta, GA. Information resulting from the STAR will be used by the Department of Defense (DoD), industry, and academia to develop an improved investment strategy for MW and MMW packaging technology. STAR emphasis was placed on the application of advanced packaging and interconnect technology to high performance phased array antennas and other complex multichip, multipackage systems. The scope of the technology encompasses array subassemblies, antenna elements, RF components, RF/digital/optical interconnects, control circuits, and thermal management of these assemblies. The subject report summarizes the information discussed at the STAR and provides recommendations for MW and MMW packaging technology investment. The STAR is an outgrowth of the AGED sponsored "Electronics Packaging" Special Technical Area Review that was held in Washington DC during 2-4 March 1992. The March meeting's focus was on microelectronic packaging technology.

As the competition for fewer and fewer DoD resources intensifies, the need for a focused MW and MMW packaging investment strategy is paramount. Hopefully, the results of the STAR will significantly aid in this definition.

III. STAR SESSION SUMMARIES

During 18-19 June 1992, 111 government, industrial, and university participants met at the Microelectronics Research Center, Georgia Institute of Technology. The STAR agenda and the list of attendees are contained in the Appendix. The STAR started with special interest presentations and was followed by four parallel working sessions: MW Multichip Module (MCM) Packages; MMW MCM Packages; MW/MMW Package Design, Modeling, and Simulation; and Military versus Commercial Packages. Within each working session, packaging problems, issues and recommended solutions were discussed and documented. The STAR concluded with a general feedback session in which the results of the four parallel working sessions were presented. Participants filled out individual feedback sheets to aid in the information collection. Copies of the special interest presentation vugraphs are contained in the Appendix. The following discussion summarizes the results of each of the four parallel working sessions. Detailed packaging technology findings and recommendations are contained in Sections IV and V of the report.

A. MICROWAVE MULTICHIP MODULE PACKAGES SESSION

The pertinent issues in the Microwave Multichip Module Packaging Session were categorized into three major topical areas: Module and/or Array Assembly, Materials, and Interconnects. Following the Session discussion and completion of the issue worksheets, the five most frequently mentioned technical areas identified as requiring additional investment were: Package materials and/or Properties Issues, Gallium-Arsenide Wafer/Die Post-Processing Properties, Standardized Packaging/ Testing Guidelines, Interconnect Issues, and Reliability Without Hermeticity Applied to GaAs/Microwave.
Each of these five areas is discussed below.

1. Package Materials and/or Properties

Better quality control and, hence, better uniformity and repeatability were the common themes in this area. Specific investigations into low temperature co-fired ceramic (LTCC), high temperature co-fired ceramic (HTCC) and metal matrix housing materials are needed. Matching the coefficient of thermal expansion (CTE) and developing housing materials with sufficient mechanical stability and heat rejection capabilities were identified as vital activities to be pursued. Included in these concerns were the observations that material interactions and outgassing/outdiffusing of incompatible materials need to be investigated. This implies a possible revision of residual gas analysis (RGA) techniques and limits to characterize the package ambient environment constituents that are detrimental to GaAs, as opposed to, or in addition to, those that have been previously determined detrimental to Si.

2. Gallium-Arsenide Wafer/Die Post-Processing Properties

The lack of data detailing/addressing the mechanical properties of processed GaAs wafers/dice, as opposed to "as sawn" GaAs wafers, was an identified concern. The need for these data are vital for determining proper CTE and CTE tolerance for GaAs die and package materials. Also included in this area is the need to characterize environmental degradation of GaAs die.

3. Standardized Packaging/Testing Guidelines

The labor intensity involved with test of die and packages and the current practice of starting from "scratch" with each package design were of great interest and importance. Also identified was the desirability of a uniform testing procedure guideline. Options
for package standardization guidelines most prevalent were a set of standard footprint housings with readily reconfigurable I/O and internal interconnect structures fabricated in a QML-like methodology. Testing issues specifically identified were determination of a uniform method of predicting channel temperature and a specification for maximum operating channel temperature.

4. Interconnect Issues

As used in this paragraph, "interconnect" applies to any of these interpretations, all of which were addressed—die-to-die within a module, module-to-module within an array, module-to-support system devices (beam former, prime power, controller, etc.), module-to-antenna element and level of integration issues. Level of integration for purposes here refers to the number of active assemblies housed within a single enclosure or housing. Also addressed in this topic was the partitioning of the system, i.e. location of common elements of the entire assembly, distributed control versus centralized

control and the means to interconnect these functional units. Specific areas identified as requiring resolution are 3-dimensional interconnects allowing for both RF and DC routing in a single structure and the potential adaptation of tape-automated bonding to microwave modules. Input and output connections were a major concern.

5. Reliability Without Hermeticity applied to GaAs/Microwave

Hermeticity requirements were identified as a very major cost-driver. The desire to proceed with a "Reliability Without Hermeticity (RWOH)" study addressing the unique requirements of GaAs die and microwave frequency systems was a clear message. More data addressing GaAs susceptibility to environmental degradation are needed.

B. Millimeter Wave Multi-chip Module Packages Session

The session participants represented organizations with a moderate diversity of applications, including smart weapons, radar, and communication systems, operating at frequencies from 20 GHz to over 100 GHz. In most cases, the circuits of interest were transmit/ receive (T/R) modules configured in electronically steered phased arrays. Other applications included single aperture arrays in the transmit-or- receive-only configuration, but requiring space qualifiable components. Overall, the participants represented a cross-section of needs and applications consistent with future MMW systems and packaging requirements. The participants identified those "enabling technology elements" that are essential to the task of developing MMW packages and are generally common to most packaging efforts. It was the opinion of the group that each of these areas require additional development effort in order to fully understand the millimeter wave packaging problems and begin to realize actual hardware. The five primary technology areas identified by the session members, presented in order of importance, are discussed in the following paragraphs.

1. Substrate Materials

This subject area was intended to address the study and development of high-performance RF substrate materials. These materials would be used for RF transmission line media, MMIC chip carriers, interconnect structures, etc., and could perhaps include the base structural element for the package. The relative scarcity of empirical data on materials at MMW frequencies requires that basic research and development be performed to identify and cultivate high-performance materials. Research should be directed at identifying candidate materials that offer the appropriate fundamental electrical, mechanical, and thermal properties, while also considering the associated process and fabrication issues such as compatible metallization schemes, solders, adhesives, etc. It was agreed that the research would be best executed if conducted by industry/industry or industry/university teams and include materials suppliers and manufacturability/reliability personnel.

2. Interconnects

As circuit density grows and greater numbers of devices are included in a single package, it becomes increasingly challenging to handle electrical interconnect. This technology element is intended to focus on multilayer interconnect technologies that are used to route the multitude of control and bias signals throughout the interior of the package. RF lines may also be included in the interconnect structure as appropriate. Recent advances in both hard and soft lamination technologies

(LTCC, HTCC, polyimides) have demonstrated the potential capability of accomplishing high density routing and interconnect inside of MMIC packages. Some of these technologies also offer the possibility of elimination or reduction of wirebonds, thereby increasing reliability, improving yield, and possibly lowering fabrication costs.

It was the opinion of the participants that these multilayer interconnect technologies should be supported and possibly augmented to explore their potential uses in MMW packaging. It was suggested that industry/vendor teams be used to build demonstration parts for a small set of typical applications. Multiple contract awards and concurrent activities would permit comparisons to be made between approaches and allow outstanding performers to be identified.

3. Housing Materials and Fabrication

This element addresses the study and development of advanced materials and techniques for the construction of the package housings. Composite materials, injection molding, advanced machining, electrodeposition, etc. are to be considered. In general, it was agreed that housing technology developed for microwave and lower frequency applications can possibly be extended into MMW bands, but may require some enhancements. These enhancements, along with other issues specific to MMW packaging, such as overall dimensions and tolerances, should be the focus of new efforts. This is not intended to be a materials-only effort, rather, the fabrication of housings and the integration with RF feed throughs is the more important issue. RF windows and aperture coupling techniques should be considered. The initial research could be carried out by first constructing demonstration hardware, such as breadboards or sample housings, developed through multiple, concurrent, small contracts.

4. RF Feed Through

This technology element includes all techniques used to carry the RF signal from inside of the package to the outside, and can include hermetic connectors, microstrip feed throughs, coupling apertures, vertical coaxial vias, etc. This area is recognized as heavily application-dependant as various architectures, radiating element designs, and operating frequencies will require different feed through design selections. A consensus of the group was that basic research and analysis in feed through designs should be conducted to identify, develop, characterize, and demonstrate a pool of designs that can be utilized at MMW frequencies. Hermeticity requirements will also influence feed through performance, so both hermetic and non-hermetic designs should be developed.

The RF feed through sustains a close functional relationship with the package housing, due to its need to penetrate the housing wall with electrical signals. As a result, it was concluded that the RF feed through research should be performed in parallel with (or as part of) housing development to avoid problems during their later merging. The suggested approach for addressing the RF feed through development is to use industry/vendor teams to build demonstration parts through multiple contract awards and concurrent activities. "Systems houses" should be included to help define the overall system performance goals and technical requirements. The antenna architectures and physical spacing requirements imposed by MMW operating frequencies will likely force the development of novel feed through structures as standardized connectors become too large for use in many systems.

5. Definition of Requirements/System Architecture

This element is intended to focus effort toward the study of advanced antenna architectures, configurations, applications, and systems that will help define the MMW packaging requirements. Based on the output of these studies, the performance goals and specifications for the packages will emerge and will help to identify the critically needed technologies. Technologies common to the greatest number of applications will certainly be of highest importance, and specialized needs will be used as longer-range goals. These studies and surveys should be continuously updated to ensure efficient, non-duplicative technology development throughout the Government. It was proposed that the study teams(s) include Government technical personnel to ensure accurate descriptions of technologies and application to appropriate systems.

The above 5 technology areas were those that the working group participants felt deserved the greatest commitment of near-term resources in order to expedite MMW packaging development. Although the issues of manufacturability and reliability were not specifically itemized in the primary issues list, it was recognized that these
topics are of great importance to packaging in all respects. It was generally understood during the discussions that manufacturability and reliability development would be considered and incorporated throughout the individual technology areas.

The millimeter wave MCM STAR participants, faced with the problems of high frequency operation, brought out an important issue that deserves long-range consideration. While the industry struggles to miniaturize components, resolve manufacturing tolerance problems, and investigate a myriad of other technical issues relating to reducing package to smaller sizes, it is important to consider other alternatives and approaches. One such approach, wafer-level integration, should be addressed in the sense that photolithographic and other MMIC-oriented fabrication techniques can be used to achieve the tight tolerances on small dimensions. Packaging, as it is presently conceived, would need to be altered significantly, but the capabilities and performance of phased array components may be improved substantially.

C. MICROWAVE/MILLIMETER WAVE PACKAGE, DESIGN, MODELING AND SIMULATION SESSION

The first issue discussed in the Session was the need to define package CAD requirements with emphasis on the user perspective. The popular approach to package design is build and then test, not analyze. Package specific CAD tools are needed. Emphasis was placed on integrating package CAD with what already exists for device and circuit design/simulation, maintaining compatibility with other tools (e.g. file/data exchange protocol, etc.) and most certainly insuring "ease-of-use." Package CAD would be most valuable if it can be easily and cost effectively integrated to augment existing MW CAD and CAT capabilities.

It was noted that some very powerful electromagnetic simulation (EM) and related software already exists that might be adapted to facilitate package design. It seems possible to make significant progress in a short period of time using existing CAD tools and validated models. The ability to perform package simulations for only linear operation of circuits/ devices will be a major improvement over current capabilities. It is not necessary to include non-linear effects or simulation down to the discrete device level to strongly enhance packaging CAD. The issue here, short term,

is identifying what's out there (e.g. commercially available at the National Labs, Universities, etc.), assessing its value and applying it to microwave package CAD. Missing pieces could then be developed as part of the longer term investment plan. Also important is that the development of software should not be initiated without a commitment to data and library element validation. Modeling approaches must be validated for numerical accuracy and verified with test results.

The consensus of the Session participants was that while significant progress has been made in applying 2-D EM analysis (e.g. spectral domain, method of moments, etc.) to planar (MMIC) structures, package design requires 3-D modeling (i.e. full wave analysis). The analysis tools must be comprehensive and complete. This means support for thermal, mechanical, as well as electrical design. Electrical performance, package resonances, modes, chip interference/performance perturbation effects, parasitic coupling, transitions, radiation, etc. must be analyzed. Geometric/electromechanical structures must be analyzed to avoid circuit to package coupling, to eliminate package induced performance anomalies and waveguide modes, and to allow for higher package densities. For thermal analysis, material properties affecting transient and steady state heating must be included for reliable designs.

It is very important to distinguish between the establishment of a "design" system from a "design and analysis" system. A "design" system can work from a validated database and design library with modest computer assets. A "design and analysis" system will require much more general capability and much greater computing power. An analysis system requires mesh generators and is memory and CPU intensive. Near term emphasis and requirements should be focused on developing a "design" system; a longer term, more expensive effort is required to develop a complete "design and analysis" system.

Package CAD should be accessible, useable, hierarchical, and consistent with device, circuit and system CAD. Framework for tool integration must support electrical and structural design and simulation. Variety of CAD/CAE tools/systems should be linked/integrated to reduce design to build time. An integrated design, assembly, and test database is required for analysis, simulation and product/process improvement. This includes provision for model library, design guidelines and design rule checking. A consistent internal database, i.e., object oriented database, should couple to the tools to represent the MMIC package design problem by representing properties and structure. An external relational (manufacturing) database could be accessed in "standard file format" to make use of models of specific structures, processes, experience and design requirement information. Access to well structured databases will be helpful for tradeoff analysis with respect to material-process, design-manufacturing, cost-benefit and standards information. The realization of a Package Design Advisor (PDA) concept for MMIC circuit designers would facilitate design by identifying package influence at the design stage, accessing heuristic design and other design knowledge, and design-manufacturing tradeoffs.

Access to the appropriate tools with sufficient computer resources should be encouraged in so far as proof of principal and beta testing are concerned. Suitable education and training is necessary to orient the user to what is possible and how to get results. The government can help facilitate access to substantial computer resources to demonstrate tool feasibility. It is not sufficiently clear how big the commercial market is for these tools. While commercialization is encouraged, the government is going to have to make the investment to accelerate tool availability. Design success will create and stimulate tool demand. Increased package complexity will also increase the demand for such tools. Improved productivity will accelerate tool use and stimulate increased demand.

D. MILITARY VERSUS COMMERCIAL PACKAGES SESSION

Historically, the commercial market has concentrated on producing functional equipment at the lowest possible cost, while military aspects are more concerned with high reliability. In order for the MW/MMW packaging technology to develop in a timely manner and be of benefit to military applications, the optimum time for government involvement and support of new technologies, material developments, processes, and procedures is now. As stated by one participant of this session, industry will continue to develop materials and technologies for commercial applications as the needs arise, but involvement and support by the government will encourage and allow packaging companies to do more advanced development while also considering military applications of the technologies being developed. If the government expects to gain any benefit from this evolving technology, military needs and requirements must be defined and support provided to second tier packaging manufacturers to pursue the advanced development efforts required to achieve low cost, military qualified packaging technologies and materials. Four major issues were identified in the military-vs-commercial packaging session. These four areas, in order of importance, are: enabling technologies, materials, standardization/QML, and modeling/simulation, and are discussed in the following paragraphs.

1. Enabling Technologies

In the area of enabling technologies, three areas were identified as most important: Reliability Without Hermeticity (RWOH), multilayer substrates, and flip-chip. RWOH is an area that is receiving attention for silicon devices in digital and lower frequency RF applications, below about 100 MHz. Development of a RWOH technology for MW applications of GaAs devices is of major importance for the government. Development of the MW technology should be developed concurrently with the current silicon RWOH efforts in order to provide a quick response to GaAs applications, rather than waiting for the silicon technology to develop. Passivation of the active area needs to be addressed for RWOH utilization, along with the development of encapsulants with tailored dielectric properties. This should be done in conjunction with a materials study/development effort to support MW RWOH. Test packages should be developed and tested to document thermal, electrical and mechanical performance and to identify any failure mechanisms.

Multilayer substrate development is another generic area for technology development. Multilayer substrates will enable dense packaging of components in modules. This technology is applicable to and may be considered an enabling technology for flip-chip, high density interconnect and conventional wirebonding. The issues to be addressed in this area include compatibility of the multilayer material with the substrate material, i.e. LTCC on AlN, or LTCC on BeO, and chip attachment to the substrate material.

In the area of flip-chip technology development, thermal modeling and thermal management need to be addressed, along with the materials and processes used for the bumps. Methods for inspection of the flipped chip and assessing the reliability of this interconnection method need to be pursued if the technology is to mature.

2. Materials

The second major area recommended for development is in materials. Investments in materials development and characterization, that is focusing on the exploitation of lower cost materials for sophisticated applications, will accelerate industry's development of affordable military packages.

Also, government focus and vision of future military packaging requirements will aid package manufacturers in prioritizing new materials studies and developments. While new materials development is always a consideration for low cost housings, test and evaluation of certain existing materials for military and commercial applications must be performed to verify their performance and reliability. In conjunction with a MW RWOH program, the development of low loss, low dielectric constant encapsulants for microwave applications is critical. A RWOH cannot succeed without a usable encapsulant. Also, investigations of existing materials such as: combined ceramics, i.e., LTCC/AlN or LTCC/BeO, utilization of inexpensive silver based inks and films for military applications and the adhesive materials for attaching GaAs on AlN are important for low cost MW/MMW packages. It is necessary to address the application of premolded, liquid crystal plastics and post molded encapsulants for military use and the further development of metal matrix and electroformed composites.

3. Standardization/QML

Package standardization and package process and test standardization is an area where the military can benefit from commercial approaches. Standardized "methods of design" data bases, doing product qualifications, process certifications and test methods are needed for industrial open architecture and transportability. Military product qualification methodology needs to be more akin to commercial procedures, and the government should explore the reliability of MIL qualified parts versus commercially qualified parts. Quick evaluation procedures or generic process qualification that is product transparent is needed and may be extended to supplier qualification. The development of a consortium should be considered to address the issues of defining packaging and reliability standards and the formation of a database of standardized design methods. The further development of a standard package database would go a long way in reducing the NRE associated with the design, testing, and qualification of specialized package outlines. Standard package outlines would allow standardized test fixtures to be developed, thus aiding in the evaluation process and greatly reducing NRE costs. Whether or not a standard package outline database can be defined, a standardized database of the materials, process and methodologies would allow for the qualification of these processes and methodologies, rather than subjecting all package designs to full verification testing. However, the military must be prepared to revise its qualification standards.

4. Modeling/Simulation

Whether it be for military or commercial applications, improved modeling/simulation tools need to be developed for MW/MMW packages. Integrated electrical, thermal, and mechanical modeling capabilities on a workstation type platform will allow more of the package analysis to be performed prior to actual hardware fabrication and concurrent engineering resulting in rapid turn around and lower cost prototypes. Additions to currently available software need to allow for modeling of the complete package, including the hosing, substrates, and interconnections, with a combined mechanical, electrical, and thermal analysis capability. Distinctions between "design" system versus "design and analysis" systems development, as discussed in Section III,C, apply here as well.

The applications of microwave and millimeter wave components is increasing in both the military and commercial market. The commercial approaches of short design cycles with rapid iterative solutions, and reliability engineering must be reviewed for military applications. This technology is just beginning to evolve, and the time is right for a commercial/military consortia to

discuss and address common needs. Also, there must be more involvement of second tier suppliers in the early stages of systems development to have them address the specifics of the package design, manufacturing, and reliability. Support for the domestic package suppliers is also a concern, and considerations should be given to promoting technology development and standardization through them. The commercial market will continue to develop low cost materials and processes for MW/MMW packages; government involvement and support can insure that developments will continue on a timely schedule and future military requirements can be addressed by newly emerging technologies.

IV. TECHNOLOGY FINDINGS AND RECOMMENDATIONS

A. MATERIALS

Under the general heading of materials are the findings related to die packaging materials, module housing materials, die bonding materials, procedures for using these materials and properties of GaAs die.

The range of packaging materials in use today is so varied that few findings are of general utility. To some extent, the material of choice appears to be somewhat site specific (experience dependent) and definitely application specific. The spectrum of package housing materials ranges from machined metal (at least 6 different metals) to ceramics (6-7 different types), ceramic walls combined with metal matrix bases (a dozen or so different matrix types) and plastic (currently exclusively used in non military packaging). Die attach media include a number of metal alloys as well as "glues" such as epoxy. Package assembly processes vary with material although "integrated" module housings formed as low temperature cofired ceramic (LTCC) or high temperature cofired ceramic (HTCC) processes are finding increasing use in prototype systems.

The mechanical fragility of GaAs die was noted to be a problem by some. It is not obvious that this "problem" is widely regarded as an issue requiring general solution. It may be more of a site specific issue than a general technology problem.

Problems of matching coefficients of thermal expansion (CTE) between base housing material and semiconductor die were frequently noted. An associated issue is the desire for a die bonding adhesive that is compliant, adheres tenaciously, is highly thermally conductive and serves to relieve stress in the die under varying thermal environments. This is a material problem that is intimately related to die fragility.

Many meeting attendees noted the critical need for a packaging materials database; i.e. a source of accurate materials data that tabulates not just individual material properties but inter-material compatibility, cost, availability, dimensional tolerances, mechanical strength, thermal properties, electrical properties at DC and microwave frequencies, outgassing (rates and species), ease of machining, ability to support soldering and brazing and ability to provide a hermetic enclosure.

While not strictly a material problem, the issue of Reliability Without Hermiticity (RWOH) received considerable attention. It was an obvious consensus position that this requirement for military packages is a major cost driver. It was felt that use of improved plastics, polymers, or other sealants that truly seal electronic circuits could eliminate the need for hermeticity and the associated and expensive hermeticity testing associated with military electronics.

RECOMMENDATIONS:

1) Develop package specifications and packaging standards.

2) Develop and maintain a materials and materials process database.

3) Investigate methods and techniques for MIL compatible RWOH for microwaves.

4) Investigate long term material characteristics; i.e. outgassing of housing and die bond materials, inter-material reactions.

B. DIE

While the only explicit die issue that was noted by multiple speakers was that of die fragility, there were a number of findings that implicitly relate to die characteristics.

There is need for more accurate methods of determining maximum die operating temperatures. There is need for more accurate ways of specifying and realizing reproducible die dimensions and for processes that will insure that specifications are met. The issues associated with RWOH have possible implications on die fabrication or post fabrication assembly processes. There is a need for die reliability specifications to be uniformly applied to MIC as well as MIMIC devices. The cost savings projected if plastic packages are employed in military hardware probably have process implications for how die are passivated and bonded.

Possibly the most significant die related finding is that there is insufficient modeling and measurement information available to allow module builders to know where and when flip-chip die attach will offer performance (including cost and reliability) benefits. Flip-chip bonding of bipolar devices is a reliable and broadly used die attach technique for digital die. This technology can probably be extended to microwave HBT die since heat generation in HBT structures is similarly located, relative to die attach locations, in HBTs and silicon bipolar transistors. The picture is less clear when FET and HEMT based die are used. Also, in the microwave domain, flip-chip die attach usually implies the use of coplanar rather than microstrip circuit designs. A coplanar circuit is generally larger in size than a comparable microstrip circuit. The overall implications for relative component cost, reliability and performance for flip-chip versus "bottom down" die are not well known.

Another finding that has die size/complexity implications is one that relates die fabrication yield, die size restrictions, die attach yield, interconnection yield and various cost factors associated with these processes. The question addressed was how to make the optimum decision on die functionality relative to module target specifications and cost requirements? For instance, in a phase combined system there will be allowable limits on module transmission phase variation as well as

other performance factors. There will also be module size and cost requirements that must be achieved. The chip foundry will generally opt for the lowest chip functionality and the smallest chip size in order to maximize chip foundry yield, but possibly at the expense of more costly assembly and packaging. The module assembler will want to purchase the fewest chips possible with the smallest performance variations in order to maximize module assembly yield and limit assembly cost. From the end users' point of view all that is required are modules that meet requirements, that provide reliable operation and that meet cost objectives. Assembly/test cost, module-module performance variation and packaging cost are usually minimized by using the highest level of integration of functionality for the chip. It would be very useful to have available a method for trading off various yield/cost/performance factors for modules that would allow suppliers and users to find more optimum solutions for module supply than is now possible.

RECOMMENDATIONS:

1) Models and methods for accurately comparing the benefits/ liabilities of using flip-chip die attach with standard "bottom" die attach.

2) A survey of module suppliers to determine whether chip fragility is a sufficiently prevalent problem to warrant serious attention.

3) Methods and techniques for accurately measuring or modeling temperature in chips is needed.

4) *Uniform reliability specification and assessment methods* are needed at the device, chip and module levels to accommodate realistic performance trade-offs.

5) Development of a yield/cost/performance model that relates chip functionality, assembly cost, package cost and module performance is needed.

C. MULTILAYER STRUCTURES

Multilayer structures, in the present context, refer to packaging structures that include LTCC housings, glass/silicon (GMIC) substrates, conformal laminates and films decorated with conductor patterns that form packaging structures when combined with rigid housing substrates. Multi-layering is associated with multifunction integration of package parts; i.e. integrated conductor patterns, vias, heat sinks, I/O ports, and in the most aggressive cases, microchannel cooling capability. In general, multilayer technology is being used in developmental programs and has not yet matured to the level that it is employed as routine practice for deployable hardware.

LTCC offers the possibilities of forming conformal housing shapes, matched CTEs, integrated heat sinks, integrated vias and multilayer interconnects and integrated RF I/O ports. However, while this technology may be the most advanced of multilayer approaches, significant issues remain to be resolved before it can be considered sufficiently mature for low cost module manufacturing. LTCC appears to be much closer to providing module housing solutions for the microwave frequency range than for MMW frequency applications.

For instance, transmission line losses are acceptable up to frequencies in the range of 40 Ghz. Above this frequency range losses become excessive. Improved metallization methods are required to reduce losses at MMW frequencies. Improved dimensional control is needed, particularly for housings used at MMW frequencies and at all frequencies where chip cavities are employed as mounting positions for die.

New testing strategies and methods are required to support accurate qualification of highly integrated module housings that result from exercise of this technology.

Similarly, better definition of end use specifications are required to guide refinement of design practices, fabrication methods, raw material tolerances, dimensional tolerances and testing routines.

Housing walls in LTCC housings are formed from multiple layers of ceramic. Housing size, for applications in phase combined systems, scales inversely with frequency. Consequently, at MMW frequencies, housing walls can become so thin that with presently available LTCC materials and processes, they are mechanically fragile.

Heat removal from LTCC modules requires introduction of high thermal conductance materials under heat generating devices. Thermal conductance can be enhanced by introduction of high thermal conductance vias or by integrating a high conductance "plug" in the ceramic base. Both technologies have been demonstrated to be effective solutions and both require refinement to become qualified for manufacturing.

An additional and or complimentary approach for thermal management is inclusion of microchannel cooling troughs within the base of the housing. This technology appears to have great potential but at this time it can only be considered to be an attractive concept.

Both LTCC and HTCC technologies require integration of I/O ports within the housing structure. RF I/O port design is not a well established engineering discipline primarily due to the lack of accurate models and CAD simulation capability. While this poses a design problem for all package types, it is a particularly serious problem for those housings formed from integrated multi-layers, like LTCC, where the I/O is an integral, non-separable part of the housing structure.

In addition to LTCC ceramic housings, multilayer structures using aluminum nitride (AlN) are being developed that provide much improved thermal conductance over conventional ceramics. This technology needs developmental work in basic materials, processes and methods of use. Also, glass/silicon multi-layers are being used to develop approaches for "wafer level" assembly of low cost, high performance multifunction modules.

"Flexible" layers also are being evaluated for use as carriers of bias and logic distribution networks. These layers can be employed in multichip modules to provide a medium that eliminates the need for wire bonded intra-module connections.

RECOMMENDATIONS:

1) Development of a "standard" specification format is needed to guide design, manufacturing and materials "tolerancing."

2) Development of improved test methods for materials used in multilayer housings and housing structures is needed.

3) Development of integral heat removal techniques and associated testing and manufacturing methods is an important need.

4) Qualified materials databases and design libraries are needed to support efficient multilayer housing design.

5) Additional work to evaluate capabilities and develop implementation technologies of newer material forms such as Aluminum Nitride (AlN), Silicon Carbide (SiC), etc. has high potential payoff.

D. HOUSINGS (METAL AND METAL MATRIX)

Findings described in this section are closely related to those found under materials and multilayer structures but have been particularized to metal matrix composites (MMC) and metal module enclosures. Further, findings are differentiated by application area; i.e. military and commercial and within the military category, microwave and MMW. The primary focus of the findings is on the fabrication processes associated with housing formation.

Housings, in the present context, pertain to enclosures that accommodate multiple chips and multiple RF functions. They will usually contain "structures'; i.e. septums, recesses, grooves, holes, etc. integral to the housing structure.

Metal housings, formed by machining, have been the de facto standard for military module housings at both microwave and MMW frequencies. For manufacturing volumes requiring less than approximately 500 production units, machining still offers lower unit cost than batch fabrication methods (at 500 units, machined metal housings can be provided at approximately 1/2 the cost of metal matrix housings while at volumes greater than 1000, composite housings are projected to provide unit costs of less than 1/5th that of machined metal).

Full metal housings can also be formed in "batch" processes such as electroforming. However, because the front end cost of mandrels is usually quite high, such processes are not yet competitive with machined housings until production volumes are large; i.e., >1000.

In current MMW military component manufacturing, metal housings continue to be the housing of choice, probably because volume production is not a driving factor. For higher MMW frequencies, where signal transmission is largely via waveguide, metal housing fabrication processes can be made compatible with integral formation of waveguide I/O ports. In the microwave regime, metal housings can be expected to play an ever decreasing role.

Commercial use of metal housings appears to be restricted to individual device enclosures; i.e. "TO cans" and MMC processes are not yet sufficiently low cost to offer acceptable commercial housing solutions.

As noted earlier in the materials section, there are many metal matrix composites under investigation and in use for prototyping applications. Processes used for forming MMC housings include pressure infiltration casting, power injection molding and metal injection molding. Each of these processes tends to be associated with particular material types and all three processes are capable of providing housings that contain structural features such as septums, recesses and grooves. With currently available technology, metal injection molding provides lowest unit cost of the three processes.

The performance drivers for composite housings include high thermal conductance and CTE's closely matched to that of GaAs (or silicon, depending on function), low RF losses, compatibility with metal coating, "adequate" control of dimensional factors (this requirement increases in intensity with increasing frequency), compatibility with hermiticity and sealing methods and high levels of mechanical rigidity. MMC material processes offer the ability to tailor many of the material features to enhance housing performance. Very low CTEs can be provided; conductivities exceeding that of copper have been demonstrated. Some of the materials are easily machined while others are very difficult to shape. Some of the materials can be formed into complex shapes by the fabrication process while others can only be formed into flat plates. All MMCs are of lower specific density than standard metals used for housings and consequently provide housing weight reductions of factors of 3-5 over comparable metal structures.

RECOMMENDATION:

Investment in methods of forming (casting, extruding, electroplating, molding, etc) complex metal matrix housings at low cost in moderate production volume is needed if these materials are to provide cost effective housings for the military market. Standardization of package outlines will allow higher volumes and enable low cost forming processes, such as casting and molding, to be used.

E. ASSEMBLIES OF MCMs (SUBARRAYS)

The findings related to manufacture of subarrays are dominated by cost issues; i.e. affordability of phase combined systems remains the dominant factor limiting application.

Specific issues remain with respect to design and fabrication of cooling manifolds. Cooling manifolds separate from the module housing are expensive to build and costly to use; i.e. connection of modules to manifolds is a labor intensive process that can directly benefit from automated assembly methods. Introduction of integral liquid cooling (or phase change cooling) into module housings can be effective in reducing production and maintenance cost of arrays.

Strategies and methods for distributing and collecting electrical signals (RF, DC bias and logic) need continuing development. Conventional methods of using "wire-wrapped" distribution networks become increasingly difficult as frequency increases or as array weight be-comes a significant performance factor. Fiberoptic techniques offer some potential advantages over

conventional distribution methods but much of the interconnect technology that will make this approach acceptable for military array use remains to be developed. The problems associated with bias and signal distribution via wire wrap become acute at the higher MMW frequencies. Also, while housing size scales inversely with frequency, connector size does not. The need for high density interconnect methods is acute in MMW phase combined arrays.

There is need for high density, reliable "plug insertion" interconnection methods for attachment of modules to array manifolds in all frequency ranges. This capability is essential if automated assembly methods are to be effective in array manufacturing.

Automated assembly processes will require a high degree of module housing mechanical integrity and reproducibility. Improved accurate but low cost methods of performing post-fabrication array testing are required.

At higher frequencies, integration of the antenna radiating element with the module housing structure can be an effective method of reducing array assembly cost.

Low cost procedures for automated, rapid and accurate conformance testing of subarrays is needed.

RECOMMENDATIONS:

1) Development of methods for design and manufacture of module cooling manifolds integral to module housings and development of "plug-in" cooling interconnects are important for reducing production and maintenance cost of active aperture arrays.

2) Strategies for implementing low loss, EMP insensitive, light weight electrical distribution networks at the array level require continuing investment.

3) Automated array assembly methods require development.

4) Automated and accurate testing methods of array performance and conformance require further development.

F. MANUFACTURING TECHNOLOGY

Findings in packaging, housing, and array manufacturing divide into three categories: equipment, support resources and methods.

Equipment issues are primarily related to the broadly based need for increased levels of assembly automation over the full spectrum of packaging, module housings and array manufacturing. There are a few examples of highly automated work stations for die attach and die interconnect existing in system manufacturing companies. In general, these systems are developmental and are too expensive to find general use throughout the component supplier organizations. Automated testing of the physical and electrical characteristics of packages, housings, and array subassemblies is needed for cost control. In the MMW frequency range, die attach and wire bonding must be

accomplished with increasing precision as frequency increases. Current automated equipment placement accuracy limits the use of automated packaging work cells to application frequencies below 40 GHz.

Needed support resources include manufacturing data base capability, statistical design methods, CAD/CAM systems particularized to packaging disciplines (see the section on CAD, below), development of standard test structures and system level analysis and synthesis capability.

New methodologies will be required to accommodate use of highly automated equipment and CAD/CAM. Much of this work will be associated with development of process models, element models; i.e. RF I/O port models, package and housing electrical models, etc.

If fiber optic interconnect technologies are to be used as feeds and interconnects in arrays, without adding to an already unacceptably high module cost level, methods for automatically assembling the optical signal parts and interface elements is required. New models will be required in order that fiber optic design can be accomplished in a packaging CAD system.

RECOMMENDATIONS:

1) Strategies for making highly automated (but high cost) packaging work cells available to commercial module vendors must be developed if these organizations are to become cost effective suppliers of modules in the emerging active aperture market.

2) Die attach equipment and wire and ribbon bonders with much improved placement accuracy are needed to support MMW module manufacturing and to improve microwave module performance reproducibility.
3) Wide scale introduction of fiberoptic interconnect technology to phased arrays will require development of automated methods for fiber handling, connection, and testing.

G. PACKAGING DESIGN, MODELING, AND SIMULATION

The need for CAD/CAM/CAT capability within the areas of package and housing design, manufacturing, assembly and test is pervasive. Current CAD practices are limited to the use of mechanical computer based design packages. Computer based simulators that will allow accurate assessment of module performance during the design phase are nonexistent. Models needed for design and simulation remain to be developed and validated. Databases of material properties, interconnect parameters, processes, transition behavior and device parameters remain to be established. Indeed, the required database implementation is not currently available.

Despite the seeming total absence of capability, the findings of the STAR are that many of the needed CAD tools exist in individual but unintegrated form and significant computer based packaging design assets can be created relatively quickly.

The required database architecture should be "object oriented" at the top level and "relational" at lower levels of the design hierarchy. The overall database can be based on currently available commercial object oriented and relational database software.

The ultimate packaging CAD system will provide the designer with the capability to perform mechanical layout of the housing assembly, allow complete simulation of overall mechanical, thermal and electrical performance, provide the ability to specify materials (BOM), processes and test procedures, provide the ability to optimize cost and performance via statistical methods and "design centering" against system level specifications and provide access to a library of validated behavioral models. Eventually, as qualified models and libraries are created and new CAD tools are formed, synthesis of full subarrays will be possible.

Mechanical design packages exist; 2D and 3D electromagnetic simulators, needed to support detailed analysis of electromagnetic behavior, exist at varying levels of utility; circuit and subsystem simulators exist; and thermal simulators exist. In order to provide a rudimentary design and analysis capability, integration of the total capability with a single "framework" that allows seamless interactive use of software tools is needed. These requirements are not dissimilar from those of the CAD portions of the MIMIC program and the MMACE activity within the Vacuum Electronics Initiative.

The principal finding of the STAR was that tool integration and database development can be initiated with currently available software and that vastly improved design capability can be provided within 1-2 years. It was also concluded that evolutionary growth, rather than a revolutionary approach, for providing the packaging industry with CAD capability was most efficient, both from a users point of view and also that of CAD system developers.

Creation of validated models and establishment of databases, essential for true design capability, is expected to be a lengthy process; i.e. essentially continuous effort for a number of years following availability of the requisite software systems.

One of the obvious and important benefits that will result from introduction of any level of useable (but accurate) packaging CAD will be the ability for the designer to perform "what if" experiments in real time. At present, development of new package designs is largely based on immediate past experience and is implemented by "cut and build" methods. Such methods are slow, labor intensive and costly. In some sense, CAD can be considered an enabling technology for housing designs that are destined for batch manufacturing since it can remove much of the risk associated with the large front end cost of mold/mandrel engineering.

RECOMMENDATIONS:

To make CAD/CAM efficiencies available to "packaging" technology, the following assets require development:

1) An accurate, comprehensive materials database that can support mechanical, electrical and thermal aspects of housing design and manufacture.

2) Integration of the following types of software tools within microwave CAD systems:

   - 2-D and 3-D geometry modelers
   - 2-D and 3-D mesh generators
   - 2-D and 3-D electromagnetic simulators
   - 2-D and 3-D geometry visualization capability
   - Thermal simulation capability

- Drafting capability
- Libraries of models
- Design database system with browsing capability
- Seamless interfacing between CAD and CAM systems
- A framework that integrates all tools and data use

3) Use of advanced techniques such as "time domain-finite difference" methodology combined with supercomputer use for high speed accurate 3D analysis and simulation.

H. TESTING

The findings associated with testing span the gamut of qualification of basic materials, characterization of parts and competed assemblies, assessment of mechanical, electrical and reliability performance and improved definition of test methods.

Each area associated with packaging requires much expanded and "standardized" data sets to guide its design and manufacturing efforts. Currently, there appear to be few if any testing standards employed in the military packaging industry.

Complete material parameters and properties are not generally available to guide the user. Data that is available does not appear in a standard format. Material properties, particularly in ceramics and matrix metal, appear to be highly variable from lot to lot and among vendors. Broadly acceptable test methodologies need to be developed to guide material suppliers as well as end users.

Reliability testing is based on accurate characterization of the thermal environment imposed on the devices contained in modules and arrays. It is currently very difficult to relate external environment parameters (temperature) to the peak temperature present at the device site. This parameter is fundamental to device, and hence array MTBF predictions. Improved techniques for measuring or simulating peak device temperature are needed to support MTBF projections.

If photonics are to become a significant part of the module and array tech base, test methods and criteria for performance and reliability testing must be developed to support parts and module qualification.

To the extent automated assembly practices are used in packaging technology, automated test procedures must be also introduced in order that the full benefit of promised cost savings are realized.

RECOMMENDATIONS:

1) Standards for testing of materials, assembly methods and various performance aspects in packaging technology require development and/or definition and acceptance. Standard test data formats are considered to be an essential part of test standards.

2) Accurate methods for determining and/or modeling peak temperature and temperature distribution requires added development.

3) Development of reliability standards and appropriate test methods to qualify photonic devices and components is needed before this technology can become an integral part of array manufacturing.

I. SPECIFICATIONS AND STANDARDS (COMMON PRACTICES)

There was strong feeling among STAR participants that all areas of packaging technology are in need of much higher levels of standardization. "Standardization" is intended to mean codification and dissemination of standard practices rather than adoption of formal standards.

RECOMMENDATIONS:

Among the findings, the following needs were identified:

1) Standard ways of describing materials and intermaterial compatibility.

2) Uniform testing procedure guidelines.

3) Standard housing footprints with configurable I/O and internal interconnects.

4) Portable reliability standards and standard reliability assessment techniques.

5) Uniform techniques for qualifying GaAs die (primarily physical properties).

6) CAD, models, and data standards to support package and housing design.

7) A standardized database for materials, processes and methodologies to support package and housing manufacturing.

8) Definition of packaging specifications that are application specific; i.e. airborne, shipboard, space, etc., but which are uniform within application areas.

V. SUMMARY INVESTMENT STRATEGY

It is widely recognized by both industry and defense technologists that electronic packaging is a key area requiring increased attention and resources. Microwave and millimeter wave multichip packaging is an emerging and enabling technology that is of great importance for both defense and commercial applications. To realize affordable MW/MMW MCMs for present and advanced systems, the following general areas of investment must be pursued: development of computer controlled manufacturing tools and processes; achievement of reliability and hermeticity requirements using advanced, novel low cost approaches; development of improved 3D computer-aided design, modeling, simulation tools; investigation of new packaging materials and structures, improved material

characterization techniques, and the creation of a detailed MW/MMW MCM materials database; and the development of advanced packaging and interconnect technology for assemblies of MCMs (e.g. subarray level). "Batch fabrication" techniques must be developed at all levels of manufacturing to significantly impact overall system affordability. Technical performance advances over and above a linear extension of current packaging technology are required to meet future system requirements that impose three dimensional size constraints, light weight, adverse thermal environments, and long mission life operation.

With ever increasing competition for fewer and fewer resources, it is very important to evolve a well thought out, focused MW/MMW MCM investment strategy. Section V,A of the report summarizes the current exploratory development (6.2), advanced development (6.3), and manufacturing technology (7.8) packaging program investment. Included in the information are programs that are under contract and those planned to start in FY93. In Section V,B, focused investment recommendations are proposed for future work. The basis for the recommendations is the STAR information contained in the Appendix of the report (STAR viewgraphs and packaging materials information tables).

A. PRESENT PACKAGING PROGRAMS

Recently completed, ongoing and planned new start FY93 MW and MMW packaging and interconnect programs are summarized in Table 2 and discussed below.

1. Advanced Microwave Packaging

The Advanced Microwave Packaging program investigated materials that had properties conducive to low cost fabrication of active aperture transmit/receive modules which are compatible with different housing configurations without expensive tooling. This effort consisted of a two phased program. The first phase evaluated a large number of materials and fabrication processes from which a single material and process was downselected to evaluate during the second phase. The material selected was AlSiC as manufactured by Ceramics Process Systems, Inc (CPS). The selection was made based on superior qualities of thermal conductivity, weight, strength and fracture toughness, coefficient of thermal expansion (CTE), cost and projected capability to produce net shape housings.

During the second phase, CPS fabricated housing bases by making SiC preforms using their Quickset™ process. These preforms were infiltrated with aluminum at PCAST in Pittsburgh PA producing and AlSiC metal matrix composite. These bases were assembled with ring frames and feedthroughs to produce the desired housing. These housings were tested to determine the quality of the part as it relates to the requirements. Two demonstration module housing requirements were selected for Phase 2, the first was a separate transmit and receive housing for X-Band applications and the second was a multichannel wideband housing. Phase 2 demonstrated the versatility of the material/fabrication system to produce housing for a wide range of requirements with low tooling costs. The material selected can be tailored to produce housings with different coefficients of thermal expansion possessing high thermal conductivity. The fabrication system demonstrated the capability to produce microwave housing with demanding dimensional tolerance. The final cost projections met the current requirements for high volume microwave housings.

Table 2. FY93 MW and MMW Packaging and Interconnect Programs.

TITLE	CONTRACT NUMBER	CONTRACTOR	GOV'T AGENCY	GOV'T POC PHONE #	PROGRAM DURATION	PGM FUNDS TYPE / $M
ADV MW PACKAGING	F33615-89-C-1024	TEXAS INST	AF - WL/ELM	FRANK LAMB 513-255-7697	36 mos.	6.3 / 1.54
PROC ORIENTED MODULE	F33615-90-C-1450	M/A-COM	AF - WL/ELM	JIM GILLESPIE 513-255-7702	18	6.2 / 0.15
MW PKG/INTERCON TECH	F33615-91-C-1743	WEST	AF - WL/ELM	FRANK LAMB 513-255-7697	36	6.3 / 2.64
MW PKG/INTERCON TECH	F33615-92-C-1016	GE	AF - WL/ELM	LOIS KEHIAS 513-255-7692	36	6.3 / 2.46
MW PKG/INTERCON TECH	F33615-91-C-1012	HAC	AF - WL/ELM	KEITH STAMPER 513-255-7656	36	6.3 / 2.9
MMW T/R MODULE	F33615-92-C-1116	BOEING	AF - WL/ELM	KEITH STAMPER 513-255-7656	36	6.2 / 1.4
MFG TECH MW/MMW MCM	N62269-92-BAA-0591	TBD	N - NAWC	JOE COLUSSI 215-441-3785	12 to 36	7.8 / TBD
MIL QUAL NET SHAPE PKGs (MIMIC PHASE 3)	N00019-92-C-0106	CPS	N - NASC	CHUCK CAPOSELL 703-692-2510	24	6.3 / 1.1
MMW PACKAGING (MIMIC PHASE 3)	DAAL01-92-C-0250	MM	A - LABCOM	LEE ROSS 908-544-2360	24	6.3 / 0.79
MIMIC PHASE 2	F33615-91-C-1784	HAC/GE	AF - WL/ELM	STEVE KISS 513-255-7696	36	6.3 / PART
MIMIC PHASE 2	DAAL01-91-C-0156	TRW/WEST	A - LABCOM	TOM BURKE 908-544-2889	36	6.3 / PART
MIMIC PHASE 2	N00019-91-C-0210	RAY/TI	N - NASC	CHUCK CAPOSELL 703-692-2510	36	6.3 / PART
AF MANTECH	F33615-89-C-5712	HAC	AF - WL/MTE	P. ELWOOD 513-255-2461	48	7.8 / PART
AF MANTECH	F33615-89-C-5705	TI/WEC	AF - WL/MTE	P. ELWOOD 513-255-2461	48	7.8 / PART
A/C & SPACE RADAR STUDY	BAA-92-32	ANRO/SAIC	DARPA - ESTO	ELIOT COHEN 703-696-2214	4	6.3 / 0.3
HI DENSITY MW PKG	BAA-93	TBD	DARPA - ESTO	ELIOT COHEN 703-696-2214	48	6.3 / TBD
MMW PACKAGING	NAS3-25864	HAC	NASA - LERC	K. SHALKHAUSER 216-433-3452	24	6.3 / 0.3
MMW MCM DEV	NAS3-25870	HOLZ	NASA - LERC	K. SHALKHAUSER 216-433-3452	24	6.3 / 0.4

2. Process-Oriented Manufacturing Module Technology

The objective of this program is to demonstrate a cost/performance effective microwave manufacturing technology for the manufacture of T/R modules that is based upon the use of a unique M/A-COM developed glass-based microwave integrated circuit (GMIC) fabrication process. The demonstration vehicle is the RF subassembly of an X-Band T/R module. GMIC technology is used as a batch process-oriented means to embed, interconnect, bias and tune the MMIC and discrete RF chip components which comprise the transmit/receive functions.

Using this technology M/A-COM expects to achieve significant cost reductions relative to the labor intensive assembly, test and tuning processes normally associated with conventional hybrid integrated circuit manufacture. The effort embodied in the program makes substantial use of many process and testing concepts currently being developed in the DoD sponsored MIMIC program (Phase 2). Three X-Band GMIC T/R modules were built, tested, and delivered to the Air Force.

3. Microwave Packaging and Interconnects For Phased Arrays

Three programs are ongoing in this technical area. The overall objective is to develop techniques that will allow for batch processing and test of T/R Modules for active array applications. All three efforts are focused on the use of a large motherstrate (motherboard) on which a set of modules will be fabricated and tested simultaneously. Without any loss in performance or reliability, this program will reduce the costs of T/R Modules and address techniques for meeting the high manufacturing volumes needed to support active array implementations of airborne, ground, and space phased array systems. Furthermore, it will be a step in evolving effective manufacturing of wafer level subarrays. Other tasks in each program are addressing thermal management issues and investigations on conformal, hermetic, coatings of GaAs based microwave modules.

Westinghouse: The Westinghouse approach is based upon using high resistivity silicon as the motherstrate. The batch processing will be compatible with standard silicon processing/handling equipment and use wafers from 3 inch to 6 inch in diameter. Holes will be etched in the host wafer for placement of pre-tested, and known good, GaAs MMICs and other module components. RF interconnects between the MMICs will use microstrip circuitry printed on the high resistivity silicon. DC and control signals interconnects will be accomplished via a large polyamide structure on which the wire traces for each module are printed. This polyamide interconnect medium is placed over the wafer, aligned and then attached. This will eliminate, or reduce, the wire bonds in the modules and increase first pass yields. It is expected that 20 transmit modules can be fabricated on a 3 inch wafer. Module tests will be performed at the wafer level and acceptable modules will be diced for assembly into housings (or the next higher assembly).

General Electric: The General Electric approach uses an Aluminum Nitrate (AlN) carrier/motherboard. In this case, the AlN is metallized and acts strictly as a carrier, i.e. there are no interconnects printed on the AlN. The pretested GaAs circuits are placed in metallized tubs etched in the AlN motherboard. All RF, DC, and control signal interconnects are made by a multilayer polyamide interconnect medium processed over the wafer. This interconnect technique is known as high density interconnect (HDI) and has been demonstrated on digital ICs and some microwave circuits. For this application, techniques to process thicker polyamide layers for the RF interconnects will be developed. Isolation of the RF, DC, and control lines will be addressed and may require processing of ground planes between each interconnecting layer. At a minimum, a three layer

polyamide interconnect structure will be needed. This program will establish the baseline process on 2 inch square wafers and evolve toward 4 inch square wafers. At least 40 complete T/R modules can be fabricated on a 4 inch square wafer. Again module tests will be conducted at the wafer level with acceptable modules diced for next higher assembly.

Hughes Aircraft Company: Hughes' approach is based upon a cofired AlN motherboard. The RF interconnects will be printed on the motherboard in a coplanar format. All MMICs will be flip chip mounted on metal pads processed on the motherboard. These techniques will eliminate the need to etch holes in the host wafer for chip placement, and eliminate all wire bonds to the brittle GaAs chips. The DC and control signals will be routed in the layers of the AlN motherboard. The initial process development will use 2 inch square wafers with wafer size increasing to 4 inch in the final program phase. The Hughes program will also address vertical RF interconnects. This will allow for RF interconnections to be made between a stack of wafers. Multi-wafer interconnects will be demonstrated by interconnecting a processed wafer of modules with a wafer on which radiating elements are printed. The vertical interconnect development will address conformal and active array implementations requiring ultra thin designs.

4. Millimeter Wave T/R Module

The Boeing millimeter wave program entails developing a 35 GHz T/R module architecture emphasizing the use of existing devices to achieve affordable high performance millimeter wave arrays. Two candidate T/R architectures (tandem substrates and tandem modules) will be investigated with tandem substrates being the preferred approach. Boeing will utilize dielectrically loaded waveguide to capacitively couple the RF signal into and out of the T/R module. Elastomeric connectors will facilitate the logic and power connections to avoid the use of solder. Boeing will also investigate two different liquid cooling schemes, Fluid Immersion and Fluid Conduit, to achieve thermal management.

5. Manufacturing Technology Microwave/Millimeter Wave Multichip Modules

Under the Navy sponsored Manufacturing Technology Program, the Naval Air Warfare Center, Aircraft Division, Warminster (NAWCADWAR) is soliciting proposal abstracts for developments in manufacturing technologies relating to low cost, high volume, high rate production of microwave/millimeter wave multichip modules. Four specific areas of interest include: (1) methods and/or equipment which will reduce the test time of microwave/millimeter wave multi-chip modules and minimize the number of dedicated test stations required for production validation of various module configurations; (2) improved substrates and interconnection methods for highly integrated modules, (3) intelligent module manufacturing for improved module yields and (4) low cost module housing. Of particular interest in assessing the impact of advances in module manufacturing technology is the technology transfer potential to other companies, the direct application of the technology to multiple microwave/millimeter wave multichip modules covering a broad range of military applications, such as: radar, EW, communications, munitions, multifunction and expendables, and the potential for dual commercial as well as military applications.

6. Military-Qualified Net-Shape Manufacturing Process for Lightweight MIMIC Packages

Present and future airborne phased array radar modules demand a cost effective and lightweight packaging solution. Requirements for both US Navy and US Air Force systems are largely common. The key system level driven module requirements are summarized as:

Lightweight	≤ 3 g/cc
High Thermal Conductivity	≥ 170 W/mK at 25°C
	≥ 130 W/mK at 125°C
Similar GaAs/Aluminum CTE	6.5 - 10 ppm/°C
Precise Dimensional Control	± 0.001 inches linear
Precise Flatness Control	± 0.001 in/in flatness

The demonstration and validation phases of both Navy and Air Force phased array radar systems require light weight package capability in the 1993 to 1994 timeframe. Ceramics Process Systems Corporation and its key subcontractors, including P-CAST Equipment Corporation, have developed and demonstrated new and innovative aluminum/silicon carbide materials and a fundamentally enabling net-shape package fabrication process. An 18 month MIMIC Phase 3 program began in July 1992 which will deliver specification compliant MMIC packages, meeting design-to-cost goals for insertion into strategic military electronic systems which are currently under development by the MIMIC Phase 2 team led by the Raytheon/Texas Instruments Joint Venture. With financial and technical support from DARPA and the US Naval Air Systems Command, this MIMIC Phase 3 program will deliver a domestic merchant packaging capability focussed on the fabrication of high performance and low cost lightweight microwave packages.

7. Millimeter Wave Packaging

Martin Marietta, a millimeter wave (MMW) weapon systems developer and producer, is under contract to produce affordable MMW packaging for MIMIC Phase 3 that meets performance and reliability requirements. Numerous approaches to produce housings, including metallized plastics, injection molded ceramics, graphite composites, and electroforming were investigated. Electroforming, a high-payoff approach to MMW packaging, was selected. Electroforming is an automatic, controlled-batch process where metals are deposited and exactly replicate the shape and features of the mandrel. The electroformed part is then separated from the mandrel as a final package. The technology is more mature (less risk) than the other new approaches and offers inherent advantages such as:

1) The housing coefficient of thermal expansion (CTE) can be matched to GaAs eliminating the need for copper-tungsten base substrates, thereby reducing assembly and rework costs;

2) Highly polished surfaces suitable for waveguide applications can be produced directly without further machining or polishing;

3) Complex, lightweight, strong, thin-walled structures can be produced to exacting tolerances; and

4) Both metallic and non-metallic inserts, such as coaxial feedthrough and waveguide windows, can be "grown" in place eliminating the need for further assembly.

Martin Marietta has developed process improvements which include zero-stress plating and pulse plating of iron-nickel for controlling CTE. Electroforming will provide additional assembly and rework savings because the waveguides are formed as part of the process. For the MIMIC Phase 3 Program, Martin Marietta is designing a generic package for Ka-Band through W-Band applications. They will optimize the electroforming process for producing housings then produce, assemble and validate the package. Also, as part of our cooperative technology transfer agreement with TRW, Martin Marietta will produce electroformed housings for TRW's W-Band receiver brassboard, and TRW will assemble and validate them. Two independent electroforming foundries will be recipients of Phase 3 technology transfer.

8. MIMIC Phase 2 - Hughes Aircraft/General Electric

Most of the MW and MMW packages needed for MIMIC Phase 2 brassboards and modules are being developed using other program or company funds. LTCC MW and metal MMW packages needed for MIMIC Phase 2 are being evaluated on the program.

9. MIMIC Phase 2 - TRW/Westinghouse

The majority of MW and MMW packages needed for the MIMIC Phase 2 program are being developed on other programs. Evaluation, under Task 8, of LTCC packages for radar missile applications is being pursued in MIMIC Phase 2.

10. MIMIC Phase 2 - Raytheon/Texas Instruments

The packaging goals for MIMIC Phase 2 technology development are to provide low-cost packaging and assembly technology for advanced device implementation. This will encompass as major objectives, low-cost and lightweight domestic housings, high density and high frequency interconnects, low stress component attachment, and CAD/CAM flexible automation.

The objective of the package development task is to establish standardized methodology and viable domestic sources leading to timely, affordable, electronics packages. Metal-injection-molding (MIM) technology was developed for W/Cu in Phase 1. During Phase 2, the TI packaging team will extend this technology to include molybdenum-copper, MoCu, matrix for lower weight in a high thermal conductivity base, and NiFe 46 alloy for low power applications. The team is also investigating aluminum infiltration of silicon carbide for module brassboards to be built at Raytheon and Lockheed Sanders.

11. Manufacturing Technology for T/R Modules - Hughes Aircraft

The program has focused on the development of X-Band LTCC module housings. Both quad-pack and single channel housings have been fabricated and tested. Gold and silver multilayer metalization schemes have been evaluated for both performance and cost factors. The overall LTCC manufacturing process have been improved.

12. Manufacturing Technology for T/R Modules - Texas Instruments/Westinghouse

The TI/WEC team has developed metal matrix housings for the F-22 radar application. Both CuMo, and AlSiC housings have been fabricated and tested at X-Band. The CuMo housings are the preferred near-term approach, while the longer term goal is to move to lower weight AlSiC housings.

13. Aircraft and Space-Based Radar System Study

The objective of this 4-month project is to have contractors define what characteristics, specifications, and requirements must be satisfied to meet the operational needs of future phased array radar systems intended for use on aircraft and space-based platforms. Particular emphasis should be placed upon determining appropriate cost drivers for the electronic (analog and digital) portions of the systems. In addition, size, width, physical configuration, power supply, thermal, electrical and mechanical constraints should be described and tabulated for both aircraft and space-based platforms. DARPA's interest is in developing an information package on cost drivers to guide future investments in solid state microwave technology. The information will be used in the planning of a subsequent 48 month program for development of high density microwave (or millimeter wave) packaging for aircraft and space-based platforms. The study should identify the anticipated key problems to be overcome in implementation of fielded aircraft and space-based phase systems.

14. High Density MW Packaging for Next Generation Aircraft and Space-Based Phased Array Radars

Fabrication of future radar systems will use flexible production lines where electronic modules performing a variety of functions and using microwave, digital, and photonics technologies will be assembled. The program objective is to develop and establish producibility of complex, light weight, and high density electronic modules. For the purpose of the effort, the intended application is active array radar systems or subsystems. These integrated assemblies, typified by a complex transmit/receive (T/R) module, must be producible in sufficient quantities and at a low enough cost to be acceptable to the radar system community. Therefore, an important aspect of this program will be the development of assembly techniques to manufacture the required modules and subsystems at low cost and in high volumes. Major program goals are: 1) reducing module cost by an order of magnitude or more at specified performance levels; 2) computer controlled manufacturing tools and processes that are flexible in their production capabilities, can respond rapidly and be available to supply modules to all domestic organizations requiring them; 3) incorporating advanced technologies to meet performance and cost requirements more effectively; and 4) meeting requirements for reliability and hermeticity using advanced, novel, low cost approaches. This will require an effort to address diverse aspects of packaging the components/subsystems. The effort, therefore, will address issues such as: materials, including advanced material/ substrate investigations; multi-layer interconnect technology which includes 3-D passive or active layer techniques; electromagnetic, thermal, mechanical, and assembly modeling; high speed testing of components, modules, subsystems; improved process controls, advanced automated assembly and manufacturing methods; standard microwave and microwave/digital packaging approaches; and system integration procedures. Maintaining performance, reliability, and survivability in harsh environments; developing reliable thermal management techniques; and demonstrating packaging which maintains structural integrity in high G-force and vibration conditions are important system level packaging requirements.

15. Monolithic Microwave and Millimeter Wave Integrated Circuit (MMIC) Packaging Technology Development

A research contract awarded by NASA's Lewis Research Center (NA53-25864) to Hughes Aircraft Company is currently studying the development of high- performance packaging operating in the 18.0 - 44.0 GHz frequency range. The objective of this program is to develop a generic, or universal packaging scheme that will permit cost-effective and timely insertion of MMIC devices into NASA communication systems. The Hughes approach uses fused silica as the RF substrate material in the package to achieve extremely low RF insertion loss well into the millimeter wave frequency band. Additionally, fused silica is being used as the seal ring or "walls" of the package in a technique that ultimately provides impedance-matched, hermetic RF feedthroughs. This development effort is presently examining packaging on a single-chip basis, while stressing performance and adaptability to a variety of MMIC device configurations and operating frequencies. The contract has yielded record insertion loss performance of less than 1.5 dB to approximately 38 GHz. The technology being developed is intended to be extendable to even higher frequencies and is applicable to other package designs.

16. Quartz/Fused Silica Multi-Chip Module Development (NASA Lewis Research Center; SBIR-II; NAS3-25870)

Under a research program with Holz Industries (now called Stratedge Corp.), San Diego CA, a millimeter wave phased array antenna module is being developed. The effort addresses packaging designed specifically for phased array antenna applications by incorporating MMIC devices, control chips, interconnect, and radiating elements in a single housing. The module is built from several layers of fused silica (polycrystalline quartz) laminated to a metal base. The structure is compartmentalized and will support four, 30 Ghz, multi-bit, MMIC phase shifters that are mounted in individual, electrically isolated cavities. A single 50-ohm microstrip transmission line serves as the RF input to the module. An on-board beam-forming network divides the RF signal into four coherent parts and routes the signal to each MMIC. Two ASIC chips are mounted in the package to receive and decode control information and route appropriate DC bias and control signals to the phase shifter MMICs. Multilayer interconnect is used to route the DC bias and control paths through via holes down to layers beneath the RF substrate. The buried traces route to the appropriate locations near the MMICs, then rise (through vias) back through the RF substrate to bonding pads located directly adjacent to the MMICs. The laminated structure is designed to incorporate either end-fire or broadside- directed radiating elements (such as aperture-coupled patches). Layers are laser machined as necessary to form MMIC recesses, cavities, and walls. Fused silica is used as the RF substrate material to achieve low insertion loss. Overall dimensions of the 4-channel module, including endfire radiating elements, are 1.0 X 2.0 X 0.1 inches.

B. PROPOSED PACKAGING PROGRAMS

In this section, proposed MW/MMW packaging investment recommendations are provided. The basis for the programs is the information presented in the Appendix of the report (STAR viewgraphs and packaging materials information tables). There are five proposed areas of investment: Materials Development and Characterization; Packaging Design, Modeling and Simulation; Advanced Structures and Interconnects; MMIC Coatings; and Manufacturing Technology of Multiple Assemblies of MCMs.

It is obvious that in many cases these five areas are interdependent and overlapping. As these recommendations for investment are developed into funded programs, tasks and areas of focus may shift. Specific information for each of the five areas is provided below.

1. Materials Development and Characterization

The lack of a comprehensive and reliable data base and data models of microwave material properties, component properties, and interface properties results in design performance problems, manufacturing defects, high costs, and extended cycle times. Many microwave material properties are either unknown or so poorly documented that property values are considered unreliable. For example, loss characteristics of substrate materials and epoxies, especially as a function of frequency, are not known. Limited data is available on thermal conductivity values and coefficients of thermal expansion as a function of temperature, particularly for composite materials. Although generally unknown, knowing the distribution of material properties is key to robust design and accurate modeling. Property distribution data is also lacking for component properties. Statistical variations in electrical values and physical properties (such as dimensions, surface roughness, and reduced fracture strength by cutting to size) of both active and passive components are largely unknown. Interface properties for component attachment and interconnect for the most part is untested and/or undocumented. Such interface properties include physical, electrical and reliability data for wire, flip chip or transmission line interconnection, and epoxy or solder attachment of components. In addition, some test methods are not standardized resulting in conflicting data and poorly documented physical property values.

The lack of knowledge of statistical variations in properties results in the inability to account for such variations in the design or manufacture of the product. Present day analysis is based on a point solution for one set of property values, and hence, does not represent or account for real life statistical variations. As a result, it is presently not possible to properly select microwave materials, components, and packaging approaches, and perform mechanical and electrical modeling and design optimization.

The information below describes an approach that can, upon completion and continued maintenance, provide the microwave suppliers an on-line data base made up of current material property values, interface data, and component data. An important enhancement of the data will be statistical distribution associated with reported values and the development of data models. A data model describes the architecture of the data structure used for storing and accessing information in a database system; i.e., the various parts of the information that describes "things" have relationships that must be adhered to if the use of the information is to properly recreate "thing" behavior, structure, performance, etc. The data model defines the data elements and their relationships. With credible data available, it will be possible for both the design engineers and the assembly engineers to predict and to control the product parameters so that defect levels can begin to approach the six sigma goals (less than four defects per million opportunities).

The work recommended for investment includes the generation of a comprehensive material data base that will be conducted in two phases. Execution of the first phase is required to establish the requirements for the second phase. The primary activity of Phase 1, described in Figure 1, is to define the materials and critical properties used in the design and manufacture of microwave products. As a result, a preliminary material data base which is based on existing data will be generated. This data base will be made available to the entire microwave community within 18 months and will serve

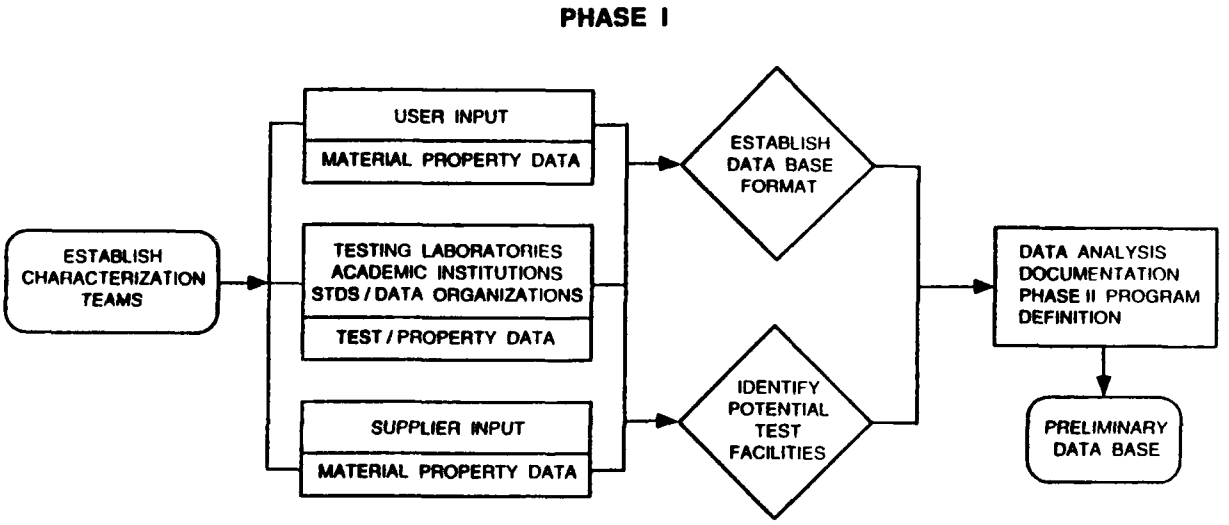

Figure 1 Flow Diagram for Establishing Preliminary Database.

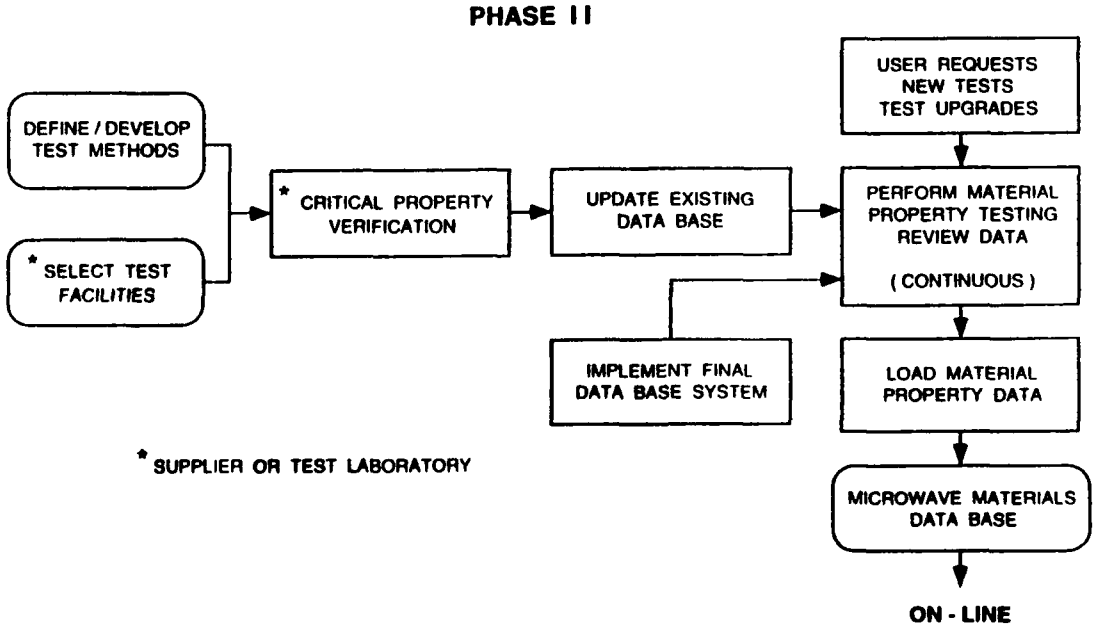

Figure 2 Flow Diagram for Test Verification and On-line Data Base.

to expand and stabilize material, component, and interface property understanding. The development of the preliminary database will also define the deficiencies and identify the testing work for Phase 2. The output of Phase 2, described in Figure 2, would be a comprehensive on-line data base of critical microwave materials, components, and interfaces.

At the completion of Phase 2, the resultant data base capability will provide a baseline integrated data base and real time communication system for critical microwave material, component, and interface properties. This capability will substantially enhance the benefits of government and industry funded efforts and result in the ability to accurately model for robust design and to manufacture at low cost and low defect levels.

RESOURCES REQUIRED: 10 person years/Yr for 4 years

2. Packaging Design, Modeling and Simulation

There is both a strong interest and a significant need for improved CAD/CAM/CAT capabilities within the areas of package and housing design, manufacturing, assembly, and test. As the density and complexity of electronic systems increase, improved CAE approaches are needed to more effectively develop affordable MMICs, MCMs, subsystems, and systems. The capability to conduct "batch fabrication" of MCMs, in which circuit and component compaction and manufacturing assembly effects are addressed, must be an integral part of the solution.

Today computer based simulators that will allow accurate assessment of module performance during the design phase are nonexistent. Models needed for design and simulation remain to be developed and validated. Databases of material properties, interconnect parameters, processes, transition behavior, and device parameters remain to be established.

The proposed investment is based upon the approach that tool integration and database development can be initiated with currently available software. An overview block diagram of the environment for MW/MMW packaging design, modeling, and simulation is shown in Figure 3. It was also determined that an evolutionary growth rather than a revolutionary approach for providing the packaging industry with CAE capability is most efficient, both from a users point of view and also that of CAD system developers. The development of a Package Design Advisor (PDA) that would facilitate design by identifying package influence at the design stage, accessing heuristic design and other design knowledge, and design manufacturing tradeoffs, is recommended.

A program consisting of 3 sequential phases is proposed. In Phase 1, user requirements will be defined and surveys/assessments of available tools (analysis & modeling, framework, databases, exchange formats, etc.) will be conducted. Case studies involving definition, application, and assessment shall be made (including the use of advanced techniques such as TDFD). In Phase 2, development and integration of tools, databases, framework models, package design advisors, etc., will be conducted. In the final phase, the developed CAE system will be evaluated by use in the design, modeling, and simulation of a broad range of MW/MMW MCMs. Tools and models will be validated and documented. Testing, to support each of the 3 program phases, is considered an important part of the effort.

RESOURCES REQUIRED: 15 person years/year for 4 years

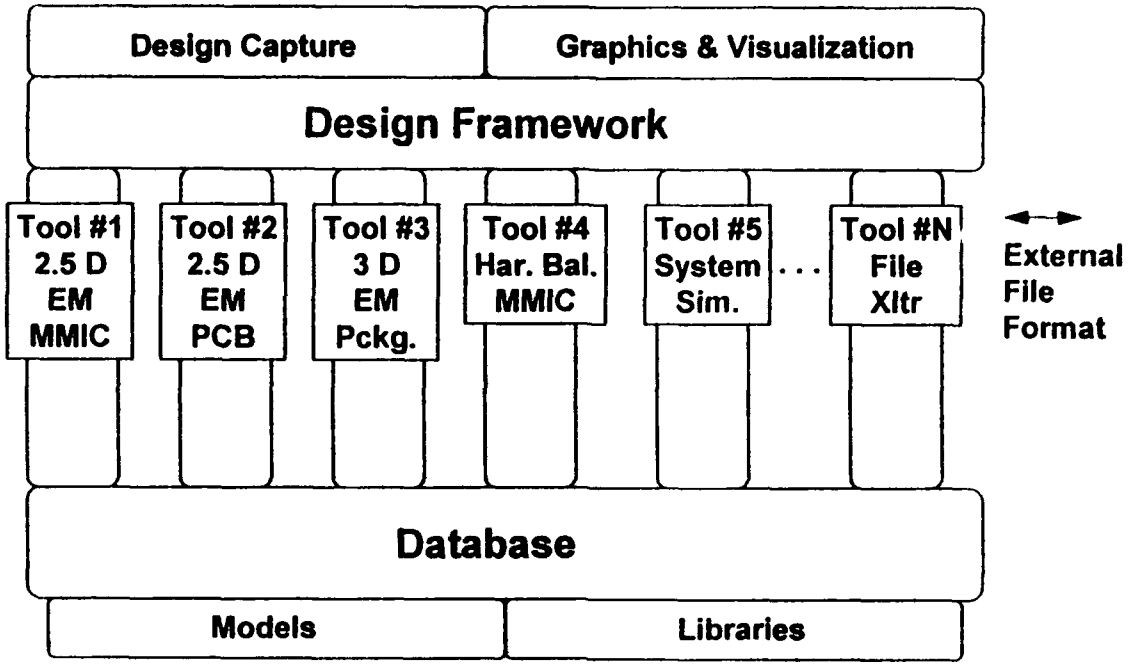

Figure 3 CAD System for MMIC, PCB, and Package Simulation.

3. Advanced Structures and Interconnects

High density and high power MW/MMW MCMs require the use of substrate and housing materials that have improved and tailorable electrical and mechanical material properties. Such materials must be suitable for use in MCM "batch fabrication" manufacturing approaches. For reasons of both increased reliability and reduced cost, improved methods of inter-MCM and intra-MCM interconnection are required. Packaging approaches should be developed and evaluated for application with the use of either upright or flip chip designs. The development of improved materials and fabrication processes must be conducted with the goal of implementing a QML manufacturing philosophy.

Three key areas of investment are recommended for Advanced Structures and Interconnects: multilayer structures, metal matrix housings, and plastic packages. Parallel multi-task efforts in each of the 3 areas will be pursued.

Multilayer structures refer to packaging structures that include LTCC, glass/silicon, conformal laminates and films decorated with conductor patterns that form packaging structures when combined with rigid housing substrates. The recommended investment in this area should be focused on the manufacturability of such structures with special focus on thermal management performance. Other development areas, such as circuit density, high conductivity internal metals, establishment of via grid, and lead pitch standards, combining different ceramics in a single structure (e.g. LTCC on AlN), and improved characterization techniques will be explored.

RESOURCES REQUIRED: 8 person years/year for 3 years per multilayer structure

Housings pertain to enclosures that accommodate multiple chips and multiple RF functions. The recommended investment is focused on methods of forming complex metal matrix composite (e.g. AlSiC and CuMo) housings at low cost in moderate production volume. Development areas include dimensional tolerancing, incorporation of feedthroughs, hermeticity, creation of certified material suppliers, and improved testing and characterization techniques.

RESOURCES REQUIRED: 8 person years/year for 3 years per MMC material

Presently, plastic commercial packages do not meet the hermeticity or performance requirements of many military applications. Ceramic packages do meet military requirements, but they are expensive for high performance assemblies. If acceptable MMIC coatings are developed, plastic packages may hold significant promise for achieving very low cost MW MCMs. The recommended investment in this area is directed at the development and evaluation of performance, manufacturing, thermal management, and environmental aspects of MW MCM plastic packages. Injection molded and premolded plastic package technology will be investigated.

RESOURCES REQUIRED: 4 person years/year for 3 years

4. MMIC Coatings

A major cost driver in military electronic packaging is the need for hermetic enclosures. Coating materials are sought for MMIC chips which provide moisture and particle protection sufficient to reduce or eliminate hermeticity requirements of the final circuit package or MCM. The recommended investment in this area is to develop and evaluate coating materials for MMIC chips. Emphasis will be placed on developing coatings that are applied at the wafer level, are compatible with MMIC processing, and compatible with a variety of housing materials (including plastic packages). MMIC performance, reliability fabrication, and cost will be evaluated for each coating approach investigated.

RESOURCES REQUIRED: 8 person years/year for 3 years

5. Manufacturing Technology for Affordable Multiple Assemblies of MCMs

An important factor in achieving affordable electronic systems is the use of an integrated CAD/CAM/CAT approach. The design and manufacturing aspects are linked among the chip, MCM, subsystem, and system levels. Performance, manufacturing, reliability, and cost tradeoffs can be effectively and quickly made to enhance the overall system. Presently, significant attention is being placed on developing chips and MCMs, but little effort is focused on the development and manufacturing technology of higher level assemblies of MCMs. For example, advanced phased array antenna systems are being developed that require thousands of MCMs. The development of design techniques and manufacturing technology for subarrays (or assemblies of MCMs) needs increased attention and investment. Complexities of RF, DC, and logic interconnections; thermal management; environmental constraints, volume limitations and light weight structural support present difficult and challenging manufacturing problems to solve. Advanced phased array antenna systems will operate over broader bandwidths, at higher powers, in more adverse environments, and possibly be conformal to the vehicle. Such requirements place even more of a need for improved design and manufacturing technology for subarray and array level assemblies in order to meet the system cost goals. The recommended investment in this area is to develop the necessary materials, design, manufacturing, and testing technologies to build subarray level assemblies of MCMs. A multifaceted program will be conducted. In Phase 1, the design of a subarray assembly will be conducted in which the

performance, thermal management, electrical interfaces, form factor weight and other critical array requirements will be determined. In Phase 2, various subarray materials, processing technologies, chips, components, interconnections, and packaging will be developed. An integral part of the work will be to develop the associated manufacturing technology needed to demonstrate subarray assembly in a high volume manufacturing environment. In Phase 3, a small number of subarrays will be built to demonstrate the subarray manufacturing technology. Performance, production, and cost assessments will be made, and designs, processes, and manufacturing equipment will be improved. In the final phase of the program, a larger number of subarray assemblies will be built in a production-like environment. Full evaluation and cost assessment of the technologies will be conducted and documented.

RESOURCES REQUIRED: 17 person years/year for 3 years

VI. REFERENCES

1. "Microelectronics Packaging Handbook," Ra R. Tamale, 1989, Van Nostrand Reinhold

2. "Microcircuit Package Stress Analysis," C. Libore, Syracuse University, RADC-TR-81-382 Technical Report, January 1982, DTIC # 820419003

3. "Strategy 2000 an Electronics Industrial Baseline Analysis Report from the Electronic Packaging Panel," R. Engall, G. Zahn, J. Fenter, Air Force/Wright Laboratory Technical Report #WL-TR-91-8032, August 1991.

4. "Handbook for Advanced MMIC Packaging," Version 1.1, Raytheon - Texas Instruments MIMIC Phase 2 Joint Venture, 14 October 1992